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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H01L 29/78 — A1

(11) International Publication Number: **WO 00/68998**

(43) International Publication Date: 16 November 2000 (16.11.00)

(21) International Application Number: PCT/US00/12261

(22) International Filing Date: 5 May 2000 (05.05.00)

(30) Priority Data:
60/132,770 6 May 1999 (06.05.99) US

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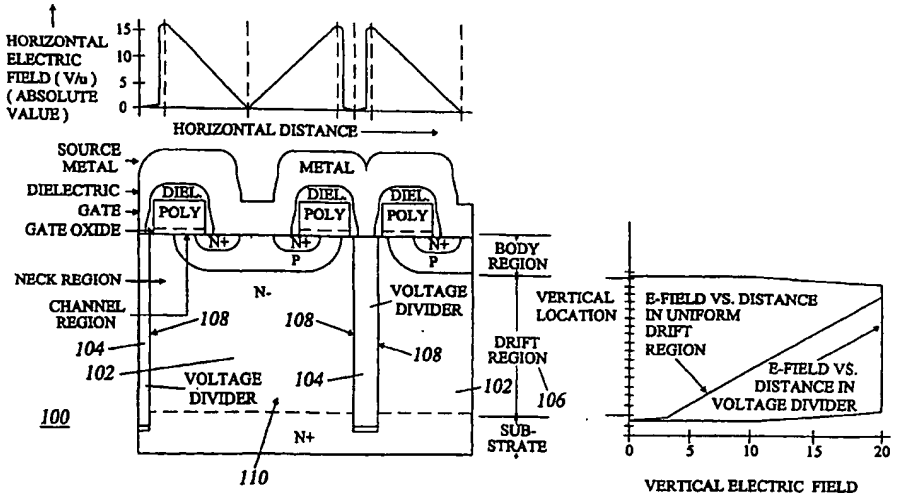
(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: HIGH VOLTAGE MOSFET STRUCTURES



(57) Abstract

A power MOSFET device that achieves low power loss characteristics by minimizing source–to–drain channel on–resistance, including a semiconductor block having a first and a second surfaces, a source region, a drain region, a drift region (106) within the semiconductor block, and a body region between the first surface and the drift region (106). The device further includes at least one voltage divider (104) disposed within the semiconductor block. The voltage divider has a first end adjacent to the first surface and electrically coupled to the source region, and a second end extending through and electrically coupled to the drain region.

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HIGH VOLTAGE MOSFET STRUCTURES

BACKGROUND OF THE INVENTION

The present invention relates to low power loss MOSFET structures, and more particularly, to low power loss MOSFET structures that achieve low power loss characteristics by minimizing source-to-drain channel on resistance.

FIG. 1 shows a cross section of the structure 10 generally used in prior art high voltage MOSFETs. Current flow through the structure is controlled primarily by the upper portion of the MOSFET structure, including the body 12, source 14, and channel regions 16, and the overlying gate element 18. The power dissipated by a high voltage MOSFET is directly related to the resistance of the path through which the device passes current. Therefore, an important design objective for such a device is minimizing the on-resistance through the structure for a given breakdown voltage. In a high voltage device, the characteristics of the lightly doped region below the body region (hereinafter referred to as the "drift region " 20) determine the breakdown voltage, and are primarily responsible for determining the device on-resistance.

The on-resistance of a device such as that shown in FIG. 1 includes three basic components. They include the resistance of the channel region, the resistance of the neck region, and the resistance of the drift region. A designer can minimize the channel and neck resistances by optimizing the structure geometry, and by shrinking pattern sizes and junction depths to the minimum values that the manufacturing process permits. In low voltage devices, the resistance of the drift region is usually small compared to the channel resistance. As the breakdown voltage increases, however, the contribution of the drift region becomes a larger part of the total. Drift-region resistance increases as $V_b^{2.4}$ to $V_b^{2.6}$ (where V_b is the breakdown voltage), because in order to support the higher breakdown voltage, the drift region must be made both thicker and of higher resistivity material. Breakdown voltage and drift region resistance are inseparably related in this type of structure because they are both controlled by the concentration of dopant atoms, and the thickness, of this region.

The drift region is uniformly doped in the horizontal direction of FIG. 1 across the entire area of the device, and is referred to herein as a uniformly-doped drift region. In the vertical direction, the dopant concentration is generally uniform, although increasing the dopant concentration toward the bottom of the drift region has been shown to reduce the drift region resistance. When the voltage applied across the device shown in FIG. 1 is such that the device is in the blocking state (i.e., no carriers flow in the channel region), an electric field (hereinafter referred to as "E-field") exists throughout the device. The breakdown voltage is dependent upon the characteristics of this E-field, and the E-field is dependent upon the dopant concentration and thickness of the drift region; thus, the breakdown voltage is dependant upon the dopant concentration and thickness of the drift region. When the device is in the blocking state, the channel is turned off so there are no carriers entering the drift region from the channel region. Under the influence of the applied voltage, the dopant atoms of the drift region lose their mobile charges and leave behind a depletion region, also referred to as a spacecharge region, consisting of (in the N channel device used as an example in FIG. 1) the fixed negative charges of the P-type dopant atoms of the body region, and the fixed positive charges of the N-type dopant atoms of the drift region. An E-field exists in the spacecharge region which varies in magnitude and reaches its peak at the junction, i.e., at the plane between the positive and negative charges. The E-field at the junction is independent of the distance between the charges, and depends only on the total charge per unit area in each region. In silicon, avalanche breakdown is known to occur when the E-field reaches a value of approximately 20 volts per micron. A charge concentration in the spacecharge region of 1.3×10^{12} electronic charges per square centimeter corresponds to an E-field of approximately 20 volts per micron, regardless of the thickness of the drift region through which these charges are distributed. But the voltage on the device corresponding to an E-field strength of 20 volts per micron is highly dependent upon the thickness of this drift region, because the voltage is equal to the integration of the E-field over the entire thickness of the spacecharge region. To achieve a higher V_b, this same quantity of dopant atoms must therefore be distributed over a thicker layer.

Drift region resistance is controlled by dopant concentration and drift region thickness because the concentration determines how many mobile charges are available to carry the current, and the thickness determines how far the mobile charges must carry the current. As noted above, the total number of dopant atoms per unit area in the drift region is approximately constant, regardless of the breakdown voltage. For a higher voltage, this same number of dopant atoms, and of mobile charges, is spread over a greater thickness. The specific resistance (resistance multiplied by area) of the drift region is equal to the resistivity multiplied by thickness of the layer. As the same number of dopant atoms is spread through a thicker layer, there is an increase in both resistivity and thickness, so the resistance increases as approximately T^2, while breakdown voltage increases as approximately T, where T represents the thickness of the drift region. As described hereinbefore, the drift-region resistance increases as $V_b^{2.4}$ to $V_b^{2.6}$ This relationship between drift-region resistance and breakdown voltage is due to the fact that carrier mobility increases as dopant concentration decreases, causing avalanche breakdown to occur at lower E-field magnitudes in higher voltage devices.

FIG. 2 shows a plot 22 of the lower limit of specific resistance for this structure with a fully-optimized dopant profile in the drift region. Even if the channel resistance and the neck resistance are reduced to zero, the on-resistance of a silicon device made with the structure of FIG. 1 can not be made lower than this value.

FIG. 3 shows a vertical channel version of a prior art high voltage MOSFET 24, also known as a Trench-MOS or U-MOS. This structure reduces both the channel resistance and the neck resistance, producing significant reductions of on-resistance in low-voltage devices, but it is of little or no benefit to high voltage devices because it still has the same drift resistance as the structure shown in FIG. 1, and so is governed by the same relationship between specific resistance and breakdown voltage.

FIG. 4 shows a prior art structure that can overcome the limits described for the structure shown in FIG. 2. This is a conductivity-modulated field effect transistor 26, more commonly known as an insulated gate bipolar transistor (hereinafter referred to as "IGBT"). The drift region 20 of this structure is subject to the same dopant concentration limits as the MOSFET structure 10 of FIG. 1, but it achieves a higher

concentration of carriers during conduction by injecting both positive and negative mobile charges during conduction. The mobile negative charges come in through the channel, just as they do in an ordinary MOSFET, but the mobile positive charges come in from the P emitter region 28 at the bottom of the structure. During conduction, the concentration of these mobile positive charges can be more than an order of magnitude greater than the concentration of the fixed positive charges, so the conductivity can be correspondingly higher, and the specific resistance correspondingly lower. When the channel is turned off the mobile negative charges stop coming in, and without these, the barrier rebuilds on the P emitter junction, causing the mobile positive charges to also stop coming in. When all these excess charges have been depleted, the device is left with the voltage supported on the same fixed positive charge distribution as in the MOSFET. Although this device has a very significantly lower specific resistance than the MOSFET, it has a major disadvantage in high frequency applications because of the time required to remove all the excess charges each time the device makes the transition from the conducting state to the blocking state.

FIG. 5 shows another prior art structure 30 which can overcome the limits of the structure 10 of FIG. 1. The structure of FIG. 5 is an example of an Alternating Conductivity Vertical Layer (hereinafter referred to as "ACVL") drift region. This structure is described in U.S. Patent No. 5,438,215, entitled "POWER MOSFET" and invented by J. Tihanyi, and also in "*A New Generation of High Voltage MOSFETS Breaks the Limit Line of Silicon*", by G. Deboy, M. Marz, J Stengl, H. Strack, J. Tihani, and H. Weber, presented December 9, 1998 at the International Electron Devices Meeting in San Francisco. A U-MOS version of this structure is described in "*Simulated Superior Performances of Semiconductor Superjunction Devices*," by Tatsuhiko Fujihira and Yashushi Miyasaka, presented at the 1998 International Symposium on Power Semiconductor Devices in Kyoto, Japan. This structure, like that of the structure shown in FIG. 4, increases the drift region conductivity by increasing the concentration of mobile negative charges. In both cases, these additional negative charges must be balanced by additional positive charges. In the

FIG. 4 structure, they are balanced by mobile positive charges, while in the FIG. 5 structure they are balanced by fixed positive charges.

The structure shown in FIG. 5 decreases the drift region resistance by placing additional N-type dopant atoms in the drift region 20 (fixed positive charges) and counterbalancing them with P-type dopant atoms (fixed negative charges) in such a way that the fixed charges neutralize each other when the device is blocking, and the N-type mobile charges participate in the current flow when the device is conducting. This neutralization is accomplished by locating the N and P type dopant atoms in alternating vertical layers 32, so that the high-voltage junction is folded up and down vertically many times across the area of the device. When the device transitions to the blocking state, the spacecharge region spreads horizontally outward from these vertical junctions. The dopant concentration in each vertical layer is kept low enough so that the layer is fully depleted before the resulting horizontal E-field is high enough to cause a horizontal avalanche breakdown. After the drift region is fully depleted by this horizontal movement, the vertical E-field continues to build up by ionizing the dopant atoms above and below the vertical layers 32. Breakdown then occurs only after the vertical E-field reaches the field strength needed for avalanche (hereinafter referred to as "critical field strength"). During conduction, the fixed charges in both the N and P vertical layers 32 are neutralized by mobile charge carriers, but only the carriers in the N type layers participate in current flow. The vertical resistance of each N layer is approximately the same, no matter what its horizontal thickness, so the lower limit for on-resistance is determined only by how thin these vertical alternating layers can be made, because this determines how many vertically-conducting layers can be placed within the horizontal area of the device.

FIG. 5 also shows the horizontal and vertical E-fields in the uniformly-doped device and the ACVL device. In the uniformly-doped device, the horizontal E-field is everywhere zero, while in the ACVL device the horizontal E-field reaches its peak values at the vertical junctions, with these peaks ideally being just below the critical field strength. In each case, the peak vertical E-field is the critical field strength, above which avalanche breakdown occurs. In the ACVL structure, the E-field remains close to this value over the entire drift region, while in the uniformly-doped

structure it decreases linearly with increasing distance from the junction. Since the integration of the E-field over the entire region (i.e., the area beneath the E field curve) represents the total voltage that the structure supports, the ACVL structure can support a higher voltage on the same drift region thickness, or equivalently, it can support the same voltage on a thinner drift region.

Although the structure shown in FIG. 5 can theoretically produce a very low specific resistance, practical shortcomings exist that limit the usefulness of the structure. The structure is inherently difficult to build, i.e., to distribute the necessary dopant atoms into these vertical layers. Another even more significant fabrication problem is that the number of dopant atoms per unit area in the vertical P layers must precisely match the number in the N layers, so that both layers deplete simultaneously. If one layer becomes fully depleted before its neighboring opposite-conductivity layer, the mobile charges in the undepleted vertical layer will allow current to flow vertically, causing an increased field at its top or bottom end, and a reduction in breakdown voltage.

Other similar structures that exhibit low specific resistance are described in U.S. patents No.5,539,238, No.5,569,949, No.5,640,034, No.5,696,010, and No.5,723,891.

It is an object of the present invention to substantially overcome the above-identified disadvantages and drawbacks of the prior art.

SUMMARY OF THE INVENTION

The foregoing and other objects are achieved by the invention which in one aspect comprises a MOSFET device, including a semiconductor block having at least a first surface and a second surface, and a drift region disposed within the semiconductor block. The drift region is characterized by a first conduction type and a predetermined dopant concentration. The MOSFET device further includes at least one body region, having a second conduction type, disposed within the semiconductor block between and adjacent to the first surface and the drift region. The MOSFET device also includes at least one source region disposed within the semiconductor block, embedded in the at least one body region so as to be adjacent to the body

region and the first surface. The MOSFET device further includes at least one drain region disposed in the semiconductor block between the second surface and the drift region, and at least one voltage divider disposed within the semiconductor block. The voltage divider has a first end adjacent to the first surface and a second end extending through the drift region into the drain region. The first end is electrically coupled to the source region and the base region, and the second end is electrically coupled to the drain region. A blocking voltage applied across the MOSFET device depletes charge carriers within the semiconductor block, so as to substantially prevent electrical current from flowing through the MOSFET between the source region and drain region.

In another embodiment of the invention, the voltage divider distributes a voltage applied across the MOSFET device uniformly over the drift region from the first surface to the drain region.

In another embodiment of the invention, the voltage divider distributes a voltage applied across the MOSFET device non-uniformly over the drift region from the first surface to the drain region.

In another embodiment of the invention, the voltage divider concentrates the voltage at the second end, proximate to the drain region.

In another embodiment of the invention, the voltage divider is selected from the group consisting of capacitive voltage dividers, resistive voltage dividers, stacked semiconductor junction voltage dividers, and combinations thereof.

In another embodiment of the invention, the voltage divider includes a resistive voltage divider characterized by one or more linear resistors.

In another embodiment of the invention, the voltage divider includes a resistive voltage divider characterized by one or more non-linear resistors.

In another embodiment of the invention, the voltage divider includes a resistive voltage divider characterized by a combination of one or more linear resistors and one or more non-linear resistors.

In another embodiment of the invention, the device further includes an edge region adjacent to the voltage divider, extending from the first surface to the drain

region. The edge region is characterized by the first conduction type and a higher dopant concentration than the remainder of the drift region.

In another embodiment of the invention, the dopant concentration of the drift region is higher along the voltage divider, relative to other portions of the drift region.

In another embodiment of the invention, a total quantity of a dopant in the drift region, when integrated horizontally from an edge adjacent to the voltage divider to a center of the region, is about $1.3 \times 10^{12}/cm^2$.

In another embodiment of the invention, the first conduction type is N-type, and the predetermined dopant concentration is such that the depletion region is substantially fully depleted at an E-field strength less than a critical field strength.

In another embodiment of the invention, the depletion region further includes a center region that is centered midway between consecutive voltage dividers, and an edge region that is substantially adjacent to the voltage dividers. The center region is characterized by a lower dopant concentration relative to the edge region.

In another embodiment of the invention, the center region and the edge region include an N-type dopant.

In another embodiment of the invention, the center region includes a P-type dopant and the edge region includes an N-type dopant.

In another embodiment of the invention, a total quantity of a dopant in the edge region, when integrated horizontally from an edge adjacent to the voltage divider to an edge adjacent to the center region, is about $2.0 \times 10^{12}/cm^2$, and a total quantity of a dopant in the center region, when integrated horizontally from an edge adjacent to the edge region to a center of the center region, is about $1.0 \times 10^{12}/cm^2$.

In another embodiment of the invention, the source region and the base region are constructed and arranged so as to form a horizontal channel region substantially parallel to the first surface.

In another embodiment of the invention, the source region and the base region are constructed and arranged so as to form a vertical channel region substantially normal to the first surface, and adjacent to the voltage divider.

BRIEF DESCRIPTION OF DRAWINGS

The foregoing and other objects of this invention, the various features thereof, as well as the invention itself, may be more fully understood from the following description, when read together with the accompanying drawings in which:

FIG. 1 shows a cross section of the structure generally used in prior art high voltage MOSFETs;

FIG. 2 shows a plot of the lower limit of specific resistance for the structure shown in FIG. 1 with a fully-optimized dopant profile in the drift region;

FIG. 3 shows a vertical channel version of the prior art high voltage MOSFET of FIG. 1;

FIG. 4 shows a prior art structure that can overcome the limits described for the structure shown in FIG. 2;

FIG. 5 shows another prior art structure which can overcome the limits of the structure of FIG. 2;

FIG. 6 shows a sectional view of one preferred embodiment of a high voltage MOSFET structure according to the present invention;

FIG. 7 shows a sectional view of an alternate embodiment of the MOSFET shown in FIG. 6;

FIG. 8 shows a sectional view of yet another embodiment of the MOSFET shown in FIG. 6; and,

FIG. 9 shows a sectional view of an vertical channel embodiment of the MOSFET shown in FIG. 6.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG 6 shows a sectional view of one preferred embodiment of a high voltage MOSFET structure 100 according to the present invention. This structure 100 decreases drift resistance in the same way as the structure shown in FIG. 5, i.e., by constructing a plurality of thin, vertical N-type layers 102 with a dopant concentration low enough to be completely depleted at an E-field strength that is less than the critical field strength. But instead of using vertical P-type layers to deplete these N-type layers 102 (also referred to herein as 'columns') when the device transitions to the

blocking state, this MOSFET structure 100 uses a plurality of vertical voltage dividers 104 ('vertical' being defined as substantially perpendicular to the surface of the semiconductor body along which the source and gate are disposed). The voltage dividers 104 may be capacitive or resistive, or a combination of both. If resistive, the voltage dividers 104 may include linear or non-linear resistors. The voltage dividers 104 may also include stacks of P-N junctions. The primary function of the voltage dividers 104 is to distribute the applied voltage appropriately over the thickness of the drift region 106, i.e., they force the depletion layer to form downward more rapidly than it would in a uniform drift region, so as to provide an approximately constant E-field over the thickness of the depletion layer. To accomplish this function, one embodiment of the invention distributes the applied voltage linearly across the dividers 104. Another embodiment of the invention may utilize the dividers 104 to concentrate the voltage near the bottom of the drift region, so as to compensate for the tendency of the such devices to concentrate the voltage near the top of the drift region.Because of the voltage distribution that the voltage dividers 104 force, this embodiment has an "E-field verses distance" profile similar to that of the ACVL device. However, the structure 100 shown in FIG. 6 does not require a critical balancing of P and N-type dopants against each other. This represents a significant advantage over the prior art. The vertical voltage profile in the divider 104 is fixed by the voltage dividing elements in it, and is independent of the dopant concentration in the adjacent silicon. In the FIG. 5 structure, negative charges (needed to compensate the positive charges of the ionized N-type dopant atoms) are provided by the ionized P-type dopant atoms, so there must be a one-to-one match of P and N dopant atoms. In the structure shown in FIG. 6, the required negative charges appear in the form of image charges within the voltage divider 104. As the N-type dopant atoms become ionized, image charges form in the voltage divider 104 in whatever quantity is required to force the vertical voltage profile in the adjacent silicon to the same voltage profile as in the divider 104, and the voltage profile in the divider 104 is fixed by the voltage-dividing elements, independent of the quantity of image charges. This redistribution of the vertical E-field allows the N^- regions to be more heavily doped for a given breakdown voltage than is possible with a uniform drift region.

An horizontal E-field also exists within the structure of FIG. 6, the magnitude of which will depend on the quantity of N-type dopant atoms. The horizontal E-field strength establishes the upper limit on the N-type conductivity, because the horizontal E-field magnitude must be kept below the critical field magnitude in order to avoid avalanche generation of carriers. The limit on the horizontal E-field magnitude thus limits the total quantity of dopant in the N^- columns 102, integrated horizontally from edge 108 to center 110, to about 1 .3 x $10^{12}/cm^2$, because this is the quantity which, when ionized, will produce a horizontal E-field of 20 volts per micron. There will also be a voltage difference horizontally from the edge 108 to the center 110 of the N^- columns 102, with the result that the depletion region is not widened as much at the centers as at the edges 108. To minimize this center-to-edge voltage difference without reducing the dopant quantity, one embodiment of the invention concentrates the N-type dopant atoms at the edges, as close as possible to the voltage dividers104, as shown in FIG. 7. The highly concentrated dopant regions are labeled N, and the less concentrated regions are labeled N--. If the total quantity of dopant in each half-column (i.e., from edge to center) is 1.3 x 10^{12} /cm^2, then the horizontal E-field at the edge will always be 20 volts per micron, and the field at the center 110 will always be zero when the column 102 is ionized. However, the horizontal voltage difference between center 110 and edge 108 will depend on how wide the column 104 is, and how the field is distributed across it. Comparing the plots of horizontal field demonstrates that if the dopant concentration is horizontally uniform across the N^- column 104, the field verses distance plot has a triangular shape, as shown in FIG. 6, and the voltage difference is equal to the area under this triangle. But if this dopant is primarily concentrated at the edges 108, as is shown in FIG. 7, the high-field portion extends only a small distance into the column 104, and the voltage difference is correspondingly reduced.

In an alternate embodiment of the invention 120, shown in FIG. 8, the N^- center of the column is replaced with a P^- region 122. This allows a further increase in the quantity of N-type dopant in the overall column (from edge to edge), because for every P-type atom placed in the center region 122, an additional N-type

atom can be placed in the edge region 124, without increasing the E-field. When the overall column is depleted, the ionized N-type atoms toward the center are electrically balanced by the ionized P-type atoms, and the ionized N-type atoms toward the edges are balanced by the image charges in the voltage dividers 104. In a fully optimized structure, each column horizontally contains 1×10^{12} P-type atoms/cm^2 in each half of the P-type portion 122, and 2×10^{12} N-type atoms/cm^2 in each of the N-type portions 124. This distribution results in a peak horizontal E-field of about 15 volts per micron outward where the vertical N-type layer 124 meets the voltage divider 104, and 15 volts per micron inward where the N-type layer 124 meets the P-type layer 122. Optimum performance occurs when the P and N dopant concentrations are matched in this way, but the presence of the voltage dividers 104 makes the structure of FIG. 8 much more tolerant of dopant variations than the prior art structure shown in FIG. 5.

In general, the structures of the present invention as described herein includes a drift region consisting of thin vertical N-type layers to carry the current over the surface of a lightly doped vertical P region. A significant difference between this structure and similar prior art structures is the inclusion of the voltage divider regions 104, which allow the N-type layers to be more heavily doped. The voltage divider regions 104 further allow the overall structure to be more tolerant of dopant variations.

The three distinct drift region architectures of FIGs. 6, 7, and 8 have been shown with the same horizontal-channel gate architecture as the structure shown in FIG. 1, but each of these drift-region architectures could also be used on a vertical-channel gate structure, of the type shown in FIG. 3. For example, a vertical-channel version of the structure shown in FIG. 6 is shown in FIG. 9. The vertical-channel version has the advantage of potentially having more vertically-conducting layers per unit area, and hence a lower on-resistance. In this structure, the same trench which is used to contain the voltage divider 104 is used to contain the polysilicon gate electrode, and the channel region is along the walls of the upper portion of the trench. In one embodiment, the upper end of the voltage divider 104 is attached to the gate electrode, as shown in FIG. 9. In alternate embodiments, the upper end of the voltage divider 104 may be isolated from the gate and attached to the source electrode.

Any of these structures can be used with a wide variety of top-surface geometries such as stripes, circles, rectangles, squares, hexagons, or other polygonal or irregular shaped patterns. The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description, and all changes which come within the meaning and range of the equivalency of the claims are therefore intended to be embraced therein.

What is claimed is:

1. A MOSFET device, comprising:

a semiconductor block having at least a first surface and a second surface;

a drift region disposed within said semiconductor block, having a first conduction type and a predetermined dopant concentration;

at least one body region, having a second conduction type, disposed within said semiconductor block between and adjacent to said first surface and said drift region;

at least one source region disposed within said semiconductor block, embedded in said at least one base region so as to be adjacent to said base region and said first surface;

at least one drain region disposed in said semiconductor block between said second surface and said drift region; and,

at least one voltage divider disposed within said semiconductor block, having a first end adjacent to said first surface and a second end extending through said drift region into said drain region, said first end being electrically coupled to said source region and said base region, and said second end being electrically coupled to said drain region;

wherein a blocking voltage applied across said MOSFET device depletes charge carriers within said semiconductor block, so as to substantially prevent electrical current from flowing through said MOSFET between said source region and said drain region.

2. A MOSFET device according to claim 1, wherein said voltage divider distributes a voltage applied across said MOSFET device uniformly over said drift region from said first surface to said drain region.

3. A MOSFET device according to claim 1, wherein said voltage divider distributes a voltage applied across said MOSFET device non-uniformly over said drift region from said first surface to said drain region.

4. A MOSFET device according to claim 3, wherein said voltage divider concentrates said voltage at said second end, proximate to said drain region.

5. A MOSFET device according to claim 1, wherein said voltage divider is selected from the group consisting of capacitive voltage dividers, resistive voltage dividers, stacked semiconductor junction voltage dividers, and combinations thereof.

6. A MOSFET device according to claim 1, wherein said voltage divider includes a resistive voltage divider characterized by one or more linear resistors.

7. A MOSFET device according to claim 1, wherein said voltage divider includes a resistive voltage divider characterized by one or more non-linear resistors.

8. A MOSFET device according to claim 1, wherein said voltage divider includes a resistive voltage divider characterized by a combination of one or more linear resistors and one or more non-linear resistors.

9. A MOSFET device according to claim 1, further including an edge region adjacent to said voltage divider, extending from said first surface to said drain region, having said first conduction type and a higher dopant concentration than said drift region.

10. A MOSFET device according to claim 1, wherein said dopant concentration of said drift region is higher along said voltage divider, relative to other portions of said drift region.

11. A MOSFET device according to claim 1, wherein a total quantity of a dopant in said drift region, when integrated horizontally from an edge adjacent to said voltage divider to a center of said region, is about $1.3 \times 10^{12}/cm^2$.

12. A MOSFET device according to claim 1, wherein said first conduction type is N-type, and said predetermined dopant concentration is such that said depletion region is substantially fully depleted at an E-field strength less than a critical field strength.

13. A MOSFET device according to claim 1, wherein said depletion region further includes a center region centered midway between consecutive voltage dividers, and an edge region substantially adjacent to said voltage dividers, said center region having a lower dopant concentration relative to said edge region.

14. A MOSFET device according to claim 13, wherein said center region and said edge region include an N-type dopant.

15. A MOSFET device according to claim 13, wherein said center region includes a P-type dopant and said edge region includes an N-type dopant.

16. A MOSFET device according to claim 13, wherein total quantity of a dopant in said edge region, when integrated horizontally from an edge adjacent to said voltage divider to an edge adjacent to said center region, is about $2.0 \times 10^{12}/cm^2$, and a total quantity of a dopant in said center region, when integrated horizontally from an edge adjacent to said edge region to a center of said center region, is about $1.0 \times 10^{12}/cm^2$.

17. A MOSFET device according to claim 1, wherein said source region and said base region are constructed and arranged so as to form a horizontal channel region substantially parallel to said first surface.

18. A MOSFET device according to claim 1, wherein said source region and said base region are constructed and arranged so as to form a vertical channel region substantially normal to said first surface and adjacent to said voltage divider.

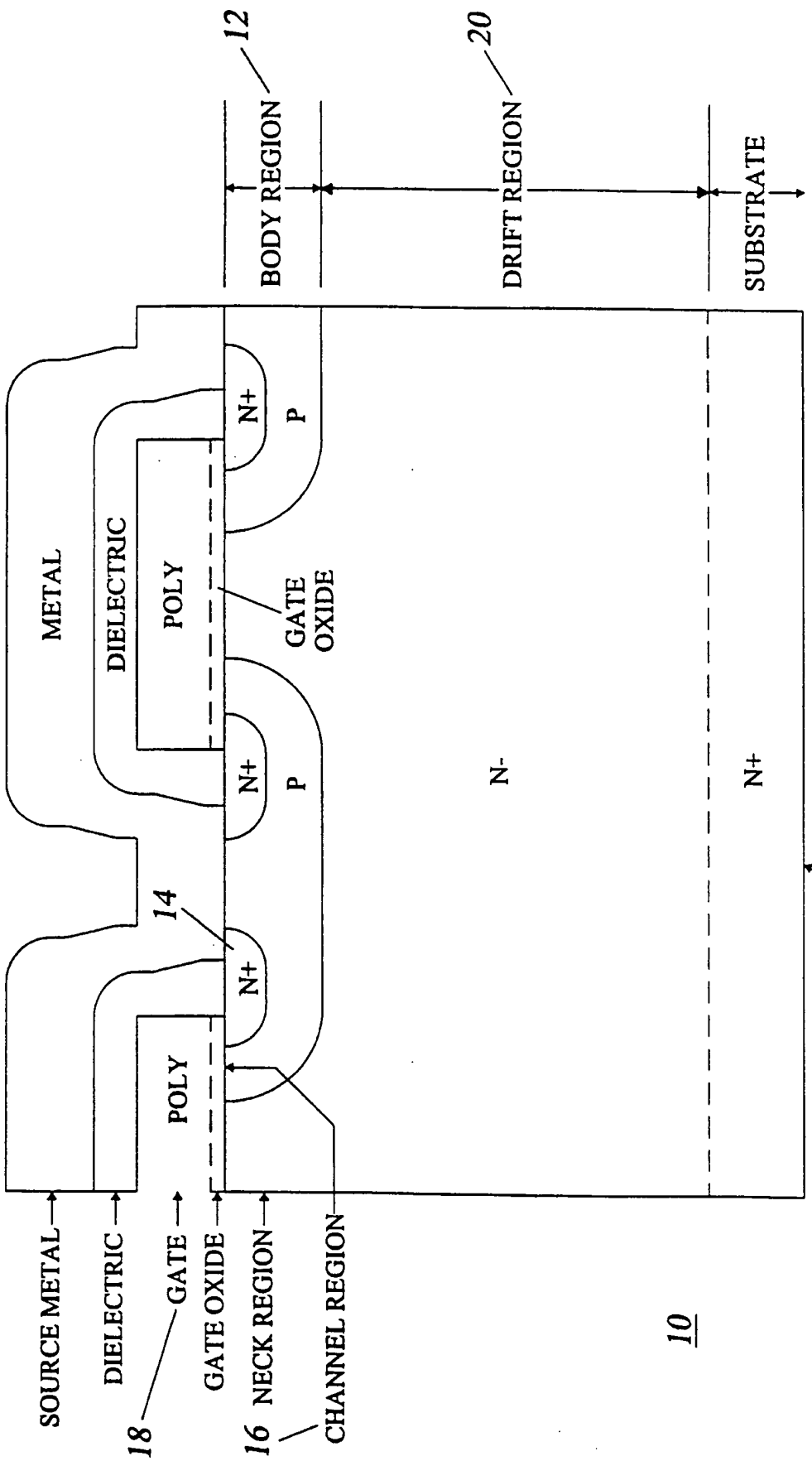


FIG. 1
(PRIOR ART)

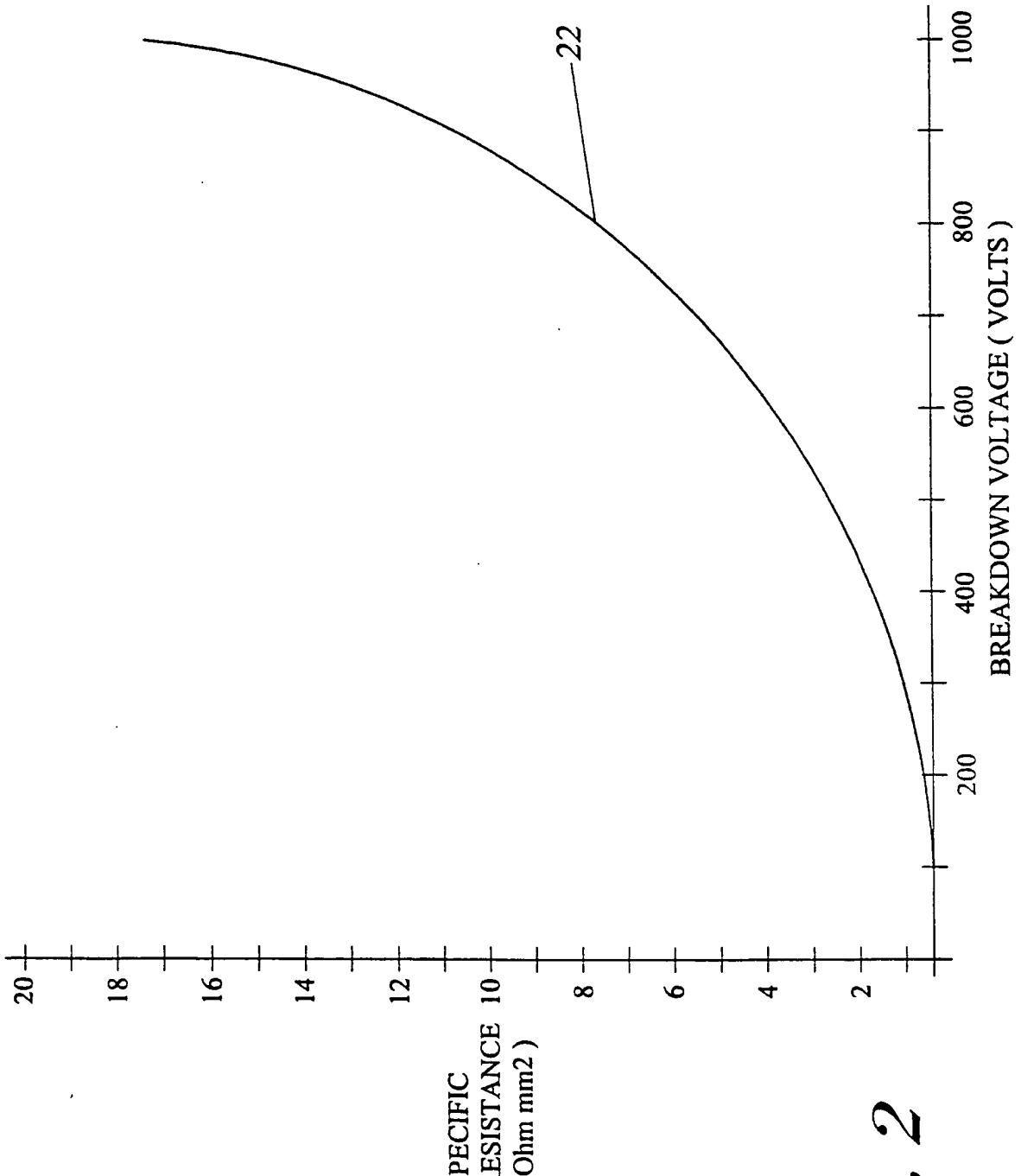


FIG. 2
(PRIOR ART)

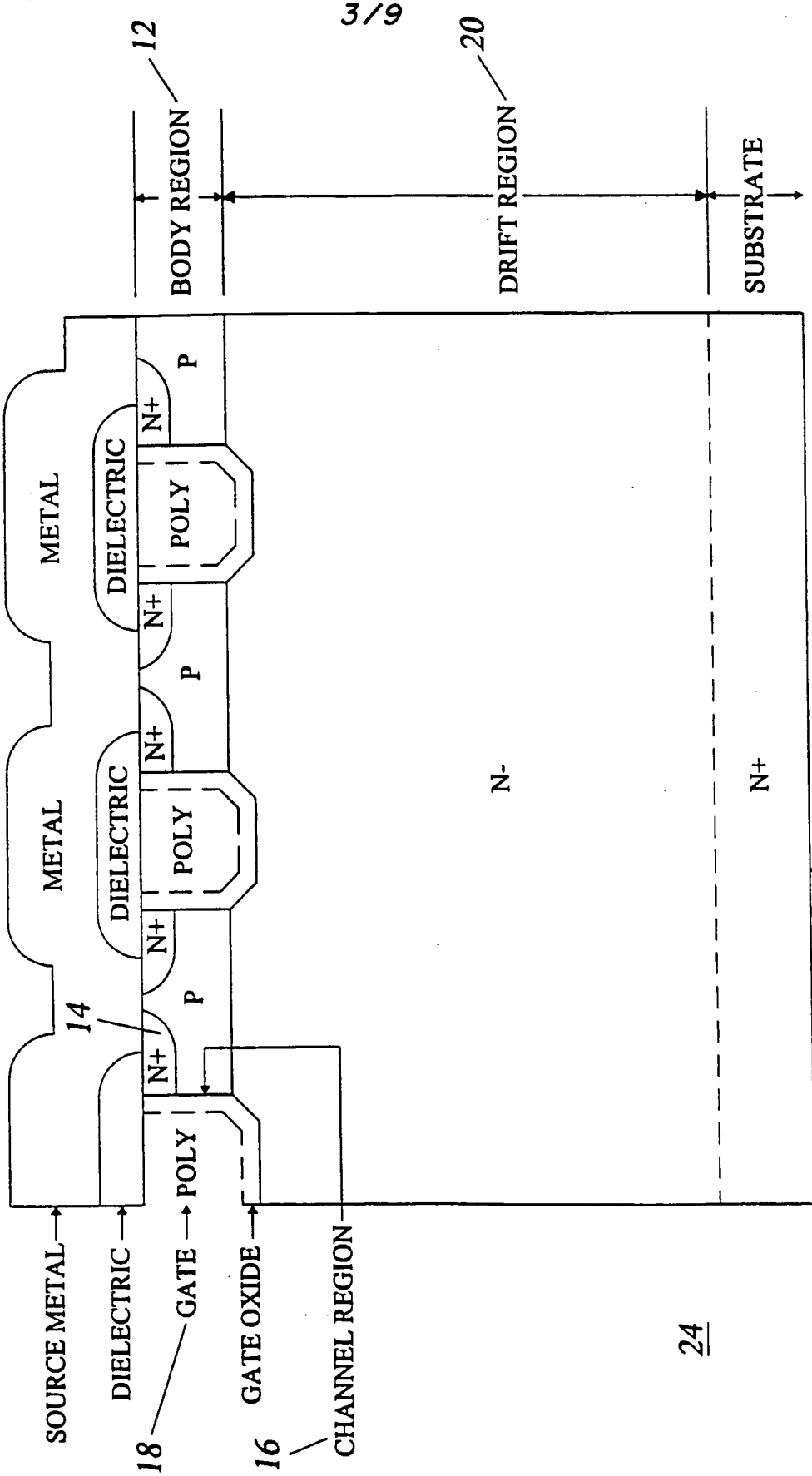


FIG. 3
(PRIOR ART)

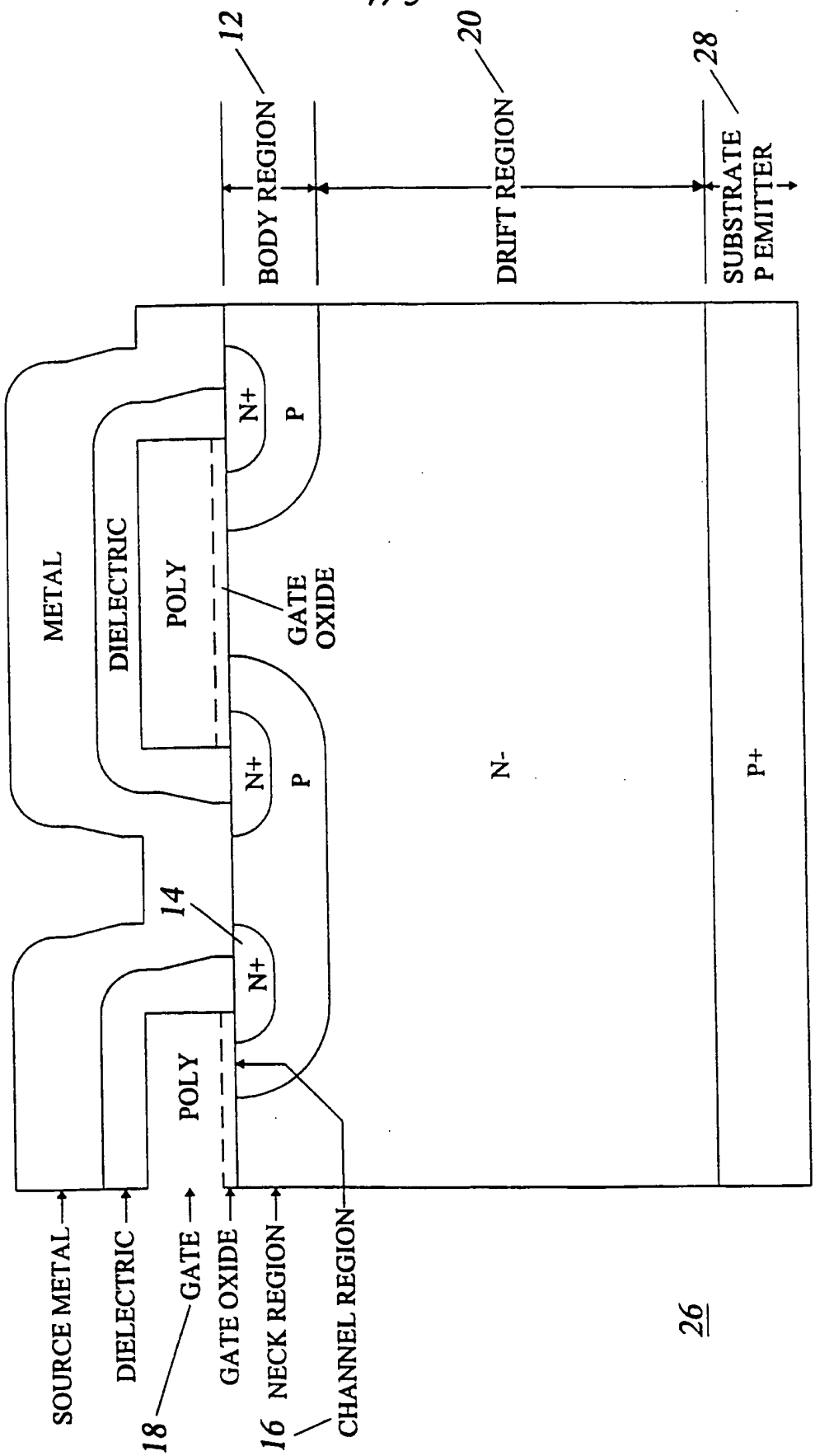


FIG. 4
(PRIOR ART)

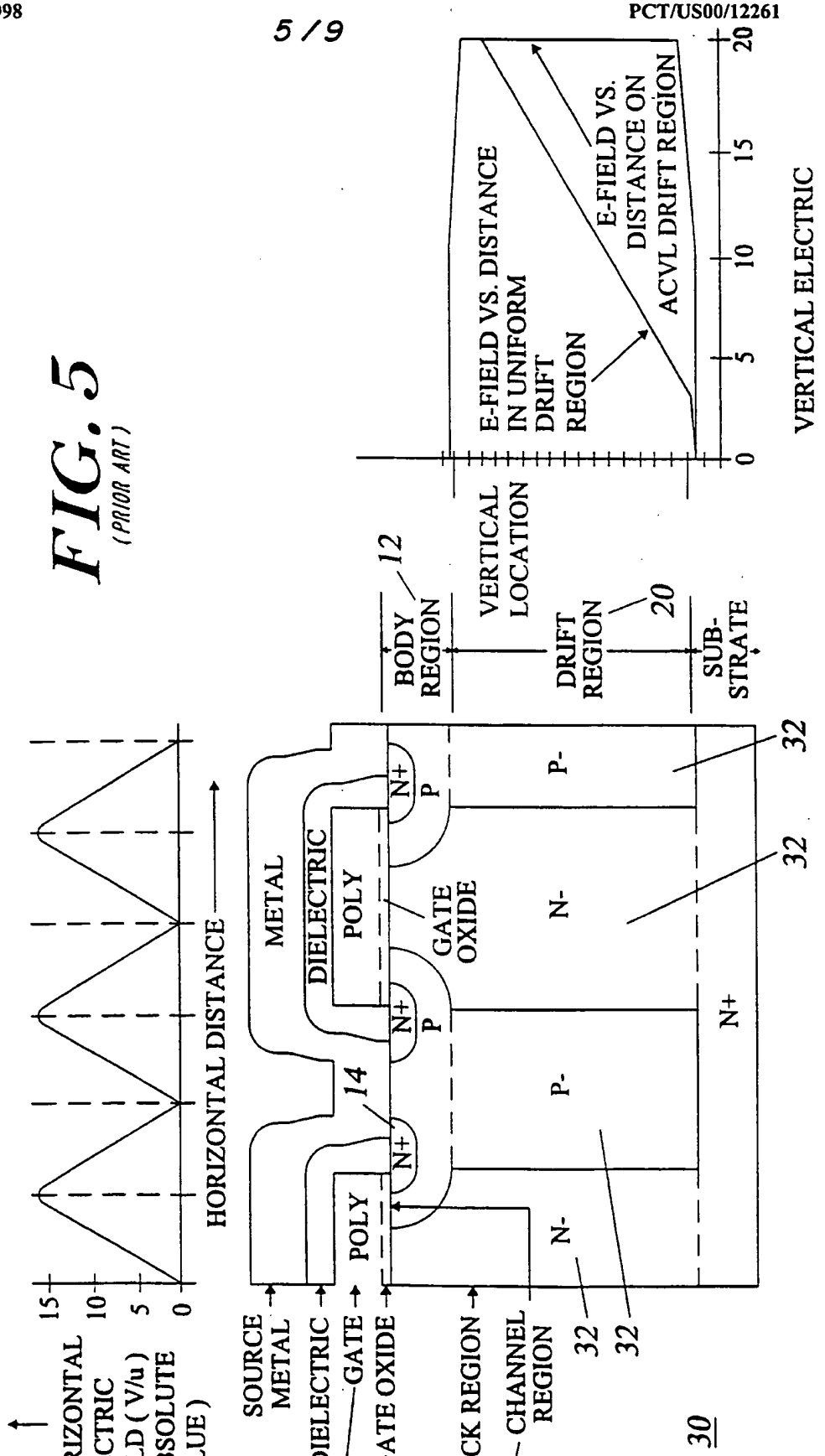
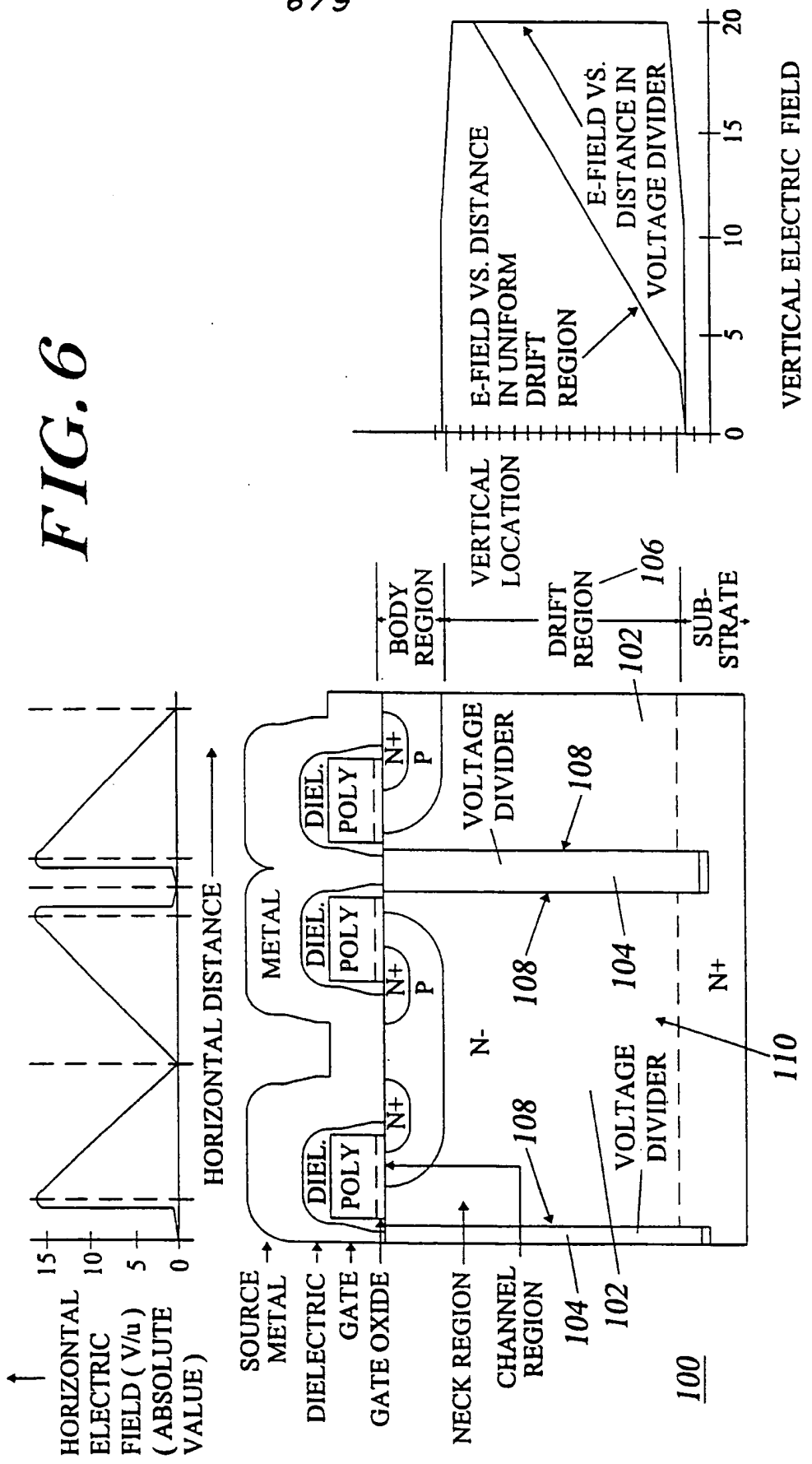


FIG. 5
(PRIOR ART)

FIG. 6


HORIZONTAL ELECTRIC FIELD (V/u) (ABSOLUTE VALUE)
15
10
5
0
HORIZONTAL DISTANCE
SOURCE METAL
DIELECTRIC
GATE
GATE OXIDE
NECK REGION
CHANNEL REGION
METAL
DIEL.
POLY
N+
P
N-
VOLTAGE DIVIDER
108
104
102
110
100
BODY REGION
DRIFT REGION
SUB-STRATE
VERTICAL LOCATION
E-FIELD VS. DISTANCE IN UNIFORM DRIFT REGION
E-FIELD VS. DISTANCE IN VOLTAGE DIVIDER
0
5
10
15
20
VERTICAL ELECTRIC FIELD

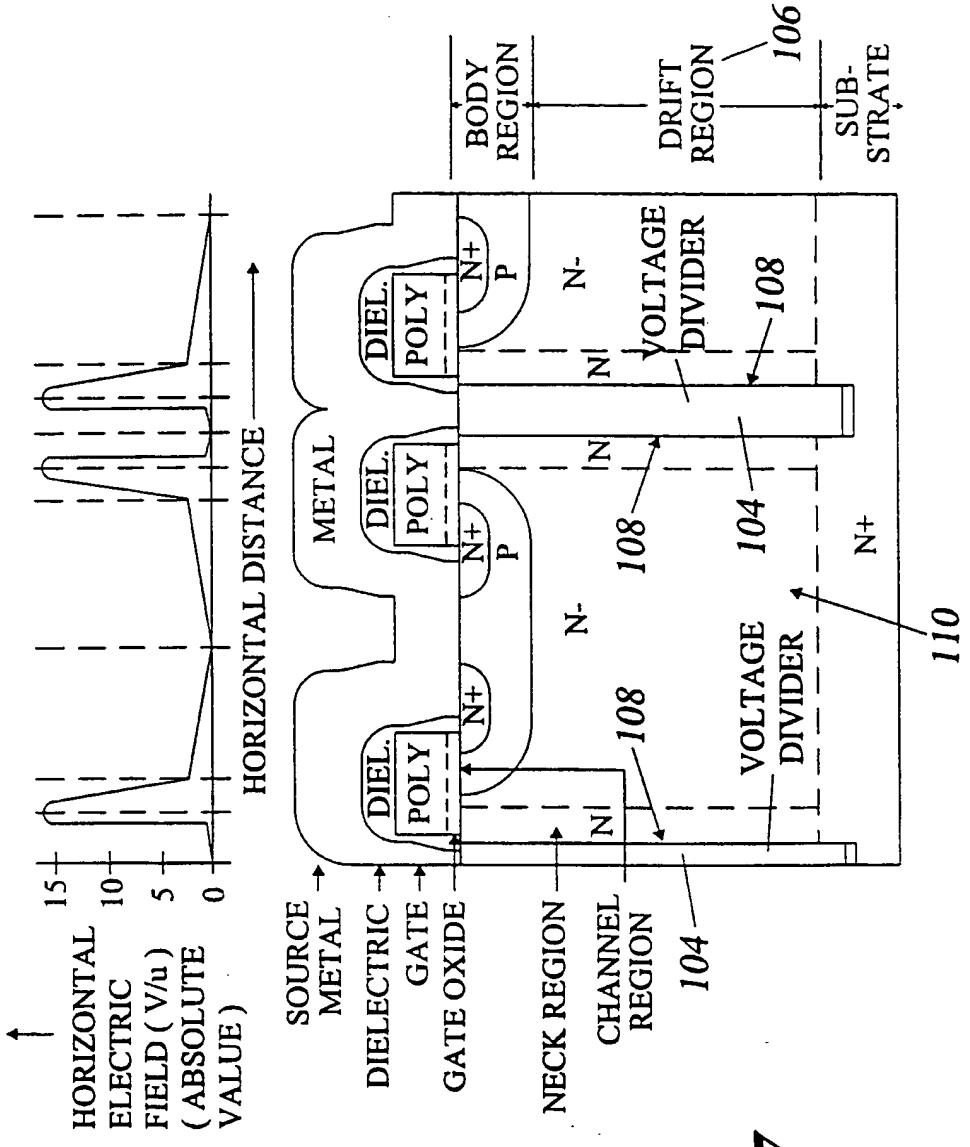

HORIZONTAL ELECTRIC FIELD (V/u) (ABSOLUTE VALUE)
15
10
5
0
HORIZONTAL DISTANCE
SOURCE METAL
DIELECTRIC
GATE
GATE OXIDE
NECK REGION
CHANNEL REGION
METAL
DIEL.
POLY
N+
P
N-
N
VOLTAGE DIVIDER
BODY REGION
DRIFT REGION
SUB-STRATE
104
106
108
110

FIG. 7

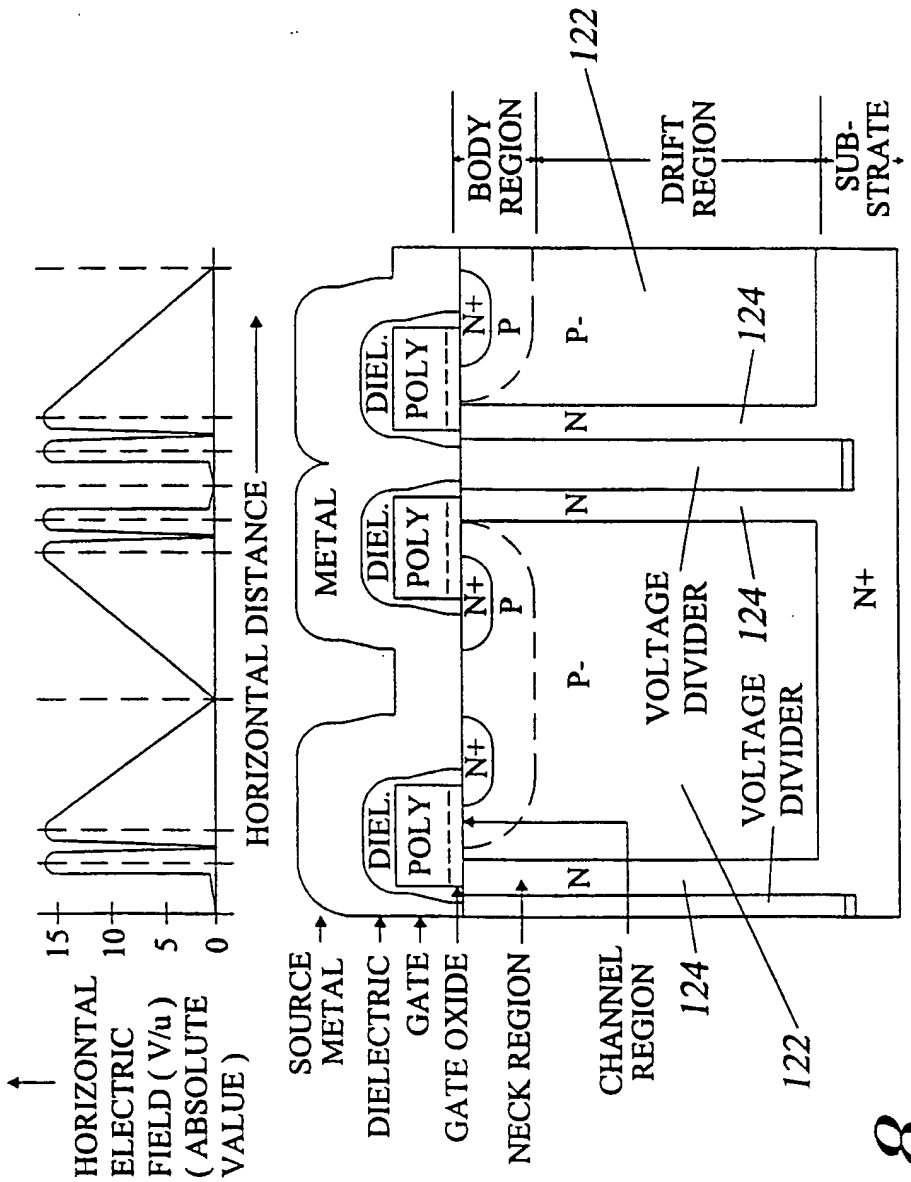

HORIZONTAL ELECTRIC FIELD (V/u) (ABSOLUTE VALUE)
15
10
5
0
HORIZONTAL DISTANCE
SOURCE METAL
DIELECTRIC
GATE
GATE OXIDE
NECK REGION
CHANNEL REGION
METAL
DIEL.
POLY
N+
P
P-
N
VOLTAGE DIVIDER
124
122
BODY REGION
DRIFT REGION
SUB-STRATE

FIG. 8

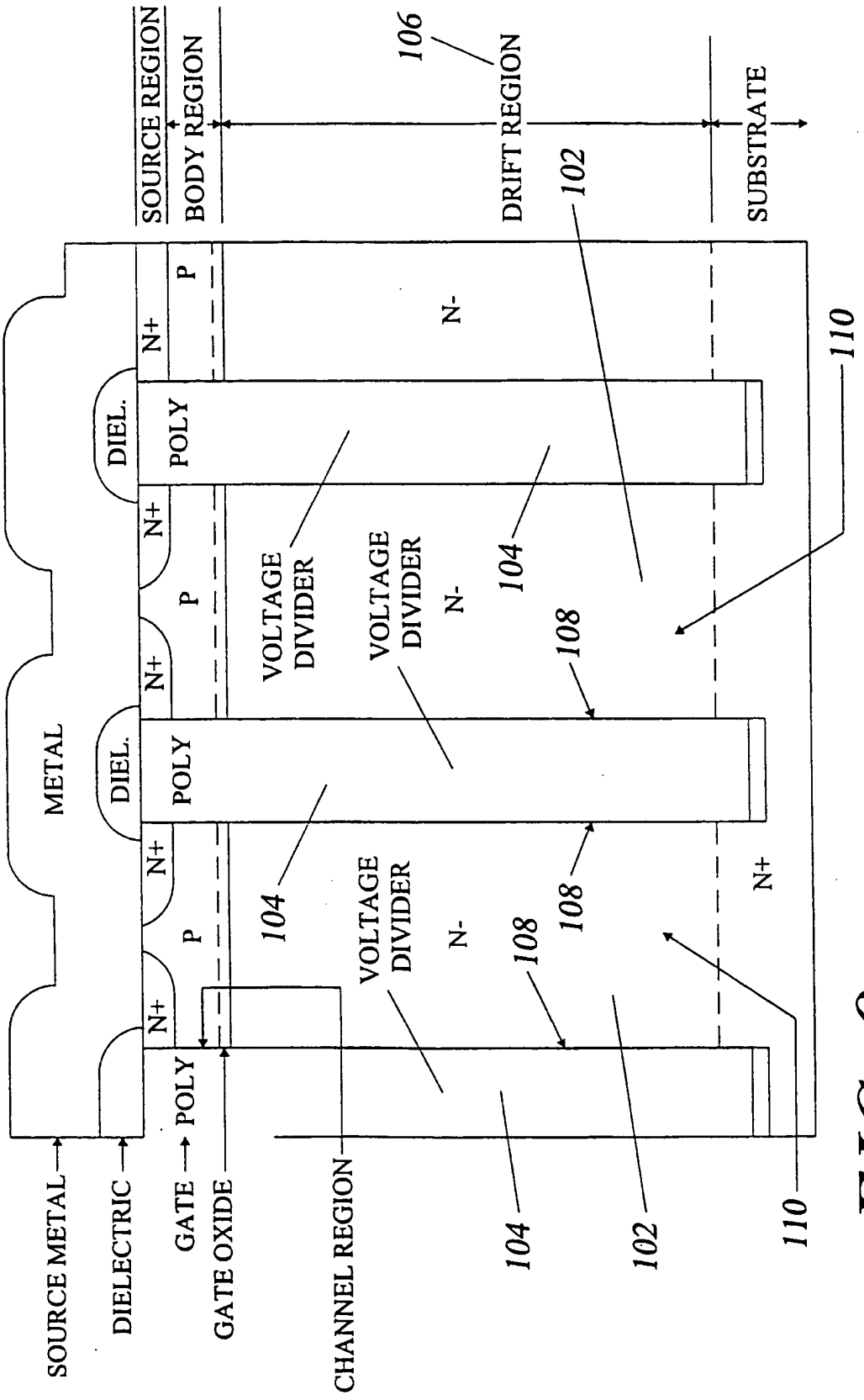

SOURCE REGION
BODY REGION
106
DRIFT REGION
SUBSTRATE
102
110
METAL
DIEL.
POLY
N+
P
N-
VOLTAGE DIVIDER
104
108
SOURCE METAL
DIELECTRIC
GATE
POLY
GATE OXIDE
CHANNEL REGION

FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/12261

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H01L 29/78
US CL : 257/342, 341, 331, 492, 493
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/342, 341, 331, 492, 493

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EAST and IEEE
search terms: power MOSFET, field distribution, voltage divider, resurf

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 5,233,215 A (Baliga) 03 August 1993 (03.08.93), col. 5, lines 10-24	1-5, 18 --- 6-17
X --- Y	US 5,438,215 A (Tihanyi) 01 August 1995 (01.08.95), col. 1, lines 26-51	1-5,18 --- 6-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 03 OCTOBER 2000	Date of mailing of the international search report 10 OCT 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer MINH TRAN Telephone No. (703) 308-0956

Form PCT/ISA/210 (second sheet) (July 1998)★